11/Pre B
J. Steptoe
3-17-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **HASHIMOTO, Hiroshi et al.** Group Art Unit: **2714**

Serial No.: **09/960,399** Examiner: **Howard Weiss**

Filed: **September 24, 2001** **P.T.O. Confirmation No.: 5652**

For. **SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS THEREOF**

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Date: March 5, 2003

Sir:

In response to the Office Action dated December 11, 2002, please amend the above-identified patent application as follows:

IN THE CLAIMS:

Cancel claim 17 without prejudice or disclaimer.

Amend claim 16 as follows:

---

16. (Amended) A semiconductor integrated circuit, comprising:

a semiconductor substrate;

B1 Cont

a non-volatile memory formed in a memory cell region of said semiconductor substrate;

a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode;

a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate